

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS ✓
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**

## **HIGH VOLTAGE LOW POWER DRIVER**

Inventor: Kushmarenko Alexander

### **FIELD OF THE INVENTION**

[001] The present invention relates generally to voltage drivers, and particularly to a high voltage low power driver, that may be used, for example, to precharge a load by a low power source and then to continue charging the load by a high voltage source.

### **BACKGROUND OF THE INVENTION**

[002] Non-volatile memory (NVM) arrays, such as erasable, programmable read only memory (EPROM) or flash memory arrays, or electrically erasable, programmable read only memory (EEPROM) arrays, require high positive or negative voltages to program and erase memory cells of the array. NVM cells generally comprise transistors with programmable threshold voltages. For example, one type of non-volatile cell is a nitride, read only memory (NROM) cell, described in US Patent 6,011,725.

[003] One procedure for programming bits, for example, in NROM cells, is by the application of programming pulses to word lines and bit lines so as to increase the threshold voltage of the bits to be programmed. After application of one or more sets of programming pulses, the threshold voltages of the bits that are to be programmed may be verified to check if the threshold voltages have been increased to a target programmed state. Any bit that fails the program verify operation may undergo one or more additional programming pulses. The sequence of application of programming pulses

followed by verification may then continue until all the bits that should be programmed have reached the target programmed state.

[004] Read and write operations may be carried out using voltages that are regulated to be above a positive voltage supply  $V_{dd}$ . The circuitry that supplies and controls the programming and verification voltages may include a high voltage driver or high voltage pump.

[005] Reference is made to Fig. 1, which illustrates a simplified block diagram of a voltage driver 10 with a model of output node. The voltage driver of Fig. 1 may include a line for input signal IN, a high voltage source HV that may be used as the source to drive the voltage, and an output line OUT that may carry the voltage from driver 10 to load 20. Output node  $n_{OUT}$  may be charged by high voltage source HV through a PMOS (p-channel metal oxide semiconductor) transistor  $P_0$  and may be discharged to ground through an NMOS (n-channel metal oxide semiconductor) transistor  $N_0$ . The drain of  $P_0$  may be connected via  $n_{OUT}$  to the source of  $N_0$ . However, the efficiency of a conventional voltage driver, such as the one shown in Fig. 1, is relatively low, reaching as low as 40%.

[006] One solution to conserve high voltage power is to precharge the output node  $n_{OUT}$  using a low voltage source prior to charging it using a high voltage source. Reference is made to Fig. 2, which illustrates a simplified block diagram of a high voltage driver 30 with  $V_{cc}$  pre charge. Components of the circuitry of Fig. 2 that are similar to that of Fig. 1 are designated with the same reference labels, and for the sake of brevity the description is not repeated. In the described high voltage driver 30 with  $V_{cc}$  precharge, a first high voltage input  $IN_1-P$  may control PMOS transistor  $P_0$  and input  $IN_1-N$  may

control NMOS transistor  $N_0$  to charge high voltage, and a second high voltage input  $IN_2$  may precharge output node  $n_{OUT}$  to  $V_{CC}$ .

[007] However, the above high voltage driver with  $V_{CC}$  precharge needs additional high voltage circuitry for generation of a second high voltage input signal  $IN_2$ , and current protection between  $V_{CC}$ , HV, and ground during switching of PMOS transistor  $P_0$ , and NMOS transistors  $N_0$  and  $N_1$ .

[008] For example, in order to open NMOS transistor  $N_1$ , which is dedicated to precharge output node  $n_{OUT}$  to  $V_{CC}$ , the voltage of input  $IN_2$  must be higher than  $V_{CC}$  plus the threshold voltage of  $N_1$ . To reach the desired voltage level, an additional voltage source, for example, HV, and a high voltage level shifter for transformation of low voltage input signal  $IN_2$  to high voltage input signal  $IN_{1-N}$  and  $IN_{1-P}$  may be used.

[009] An additional drawback of the described high voltage driver with  $V_{CC}$  precharge is the contention between HV and  $V_{CC}$ . Input signal  $IN_1$  in Fig. 2 is separated to two input signals,  $IN_{1-P}$  which is applied to the gate of PMOS transistor  $P_0$  and  $IN_{1-N}$  which is applied to the gate of NMOS transistor  $N_0$ . However, this configuration raises practical difficulties in implementation. For example, before the high voltage phase, NMOS transistor  $N_1$  has to be closed and only after it is closed PMOS transistor  $P_0$  can be open. In any other configuration  $V_{CC}$  and HV source will be shorted. Thus, the control of the switch between NMOS transistor  $N_1$  and PMOS transistor  $P_0$ , without overlapping raises an additional difficulty. The non-overlapping signals for NMOS transistor  $N_1$  and PMOS transistor  $P_0$  influence also on the time required for the switching. Therefore, this kind of driver can not be used for fast switching schemes.

[0010] In addition, practical realization of the described driver may be complicated in respect of the required silicon area, high voltage power consumed and loss of power for switching additional control signals. In addition, the described driver may suffer from other disadvantages.

[0011] Accordingly, there is a need for an efficient high voltage driver.

## SUMMARY OF THE INVENTION

[0012] According to an embodiment of the present invention, there is provided a power driver circuit comprising a low voltage source, a high voltage source, at least one input signal line, an output node, and a circuitry adapted to connect said output node to said low voltage source when said input signal line is in a first state and to said high voltage source when said input signal line is changed to a second state.

[0013] According to an embodiment of the present invention, there is provided a method to drive power from a low voltage source and a high voltage source to an output node, the method comprising connecting said output node to said low voltage source when an input signal line is in a first state and to said high voltage source when said input signal line is changed to a second state.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features and advantages thereof, may best be understood by reference to the following non limiting detailed description when read with the accompanied drawings in which:

[0015] Fig. 1 is a simplified block diagram of a voltage driver;

[0016] Fig. 2 is a simplified block diagram of a high voltage driver with Vcc pre-charge;

[0017] Fig. 3 is a block diagram illustration of a configuration of a high voltage driver in accordance with an embodiment of the present invention; and

[0018] Figs. 4 and 5 are simplified graphs of simulations of the operation of the driver of Fig. 3 in accordance with an embodiment of the invention.

[0019] It will be appreciated that for simplicity and clarity of these non-limiting illustrations, elements shown in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements may be exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals may be repeated among the figures to indicate corresponding or analogous elements.

## DETAILED DESCRIPTION OF THE PRESENT INVENTION

[0020] Reference is now made to Fig. 3 which is a block diagram illustration of a possible configuration of a high voltage low power driver 40 in accordance with an embodiment of the invention. According to an exemplary embodiment of the invention, an input signal line  $IN_1$  may be used to charge the output node with a low voltage, and an input signal line  $IN_2$  may be used to charge the output node with a high voltage. The driver 40 may have two voltage sources, low voltage source LV and high voltage source HV. In an exemplary embodiment of the invention, low voltage source LV may be tied to Vcc, and the voltage of high voltage source HV may be higher than the voltage of LV. An output line OUT may deliver the output voltage to a load.

[0021] In accordance with an exemplary embodiment of the invention depicted in Fig. 3, NMOS transistor  $N_0$  may be connected between output node and NMOS transistor  $N_1$ , and its gate may be connected to input  $IN_1$ . NMOS transistor  $N_1$  may be connected between NMOS transistor  $N_0$  and ground, and its gate may be connected to an input  $IN_2$ . NMOS transistor  $N_2$  may be connected between low voltage source LV and PMOS transistor  $P_1$ , and its gate may be connected to an input  $IN_2$ . PMOS transistor  $P_0$  may be connected between output node  $n_{OUT}$ , and high voltage source HV, and its gate may be connected to input  $IN_2$ .  $P_1$  may be connected between output node  $n_{out}$  and  $N_2$  and its gate may be connected to input  $IN_1$ .

[0022] The configuration of the embodiment of the invention depicted in Fig. 3 may allow the driver to operate in several modes, including, for example, a low voltage mode, a high voltage mode, and an efficient discharge. The operation of an exemplary embodiment of the invention is



explained in detail below; however, it will be understood by those of skill in the art that the invention is not limited in respect of the operation of the embodiment explained further below.

[0023] Reference is made to Fig. 4, which is a simplified graph of a simulation of various signals involved in the operation of the driver of Fig. 3 over time, in accordance with an embodiment of the present invention.

[0024] As indicated at  $t_0 - t_1$  in Fig. 4,  $IN_1$  and  $IN_2$  may be non-activated, setting driver 40 to an off mode, in which substantially no voltage is sourced to the output node  $n_{OUT}$ , and any voltage stored in output node  $n_{OUT}$  may be discharged and grounded through NMOS transistors  $N_0$  and  $N_1$ .

[0025] When input signal  $IN_1$  is switched ON and  $IN_2$  remains OFF, output node  $n_{OUT}$  may be pre-charged to approximately the voltage of LV through NMOS transistor  $N_2$  and PMOS transistor  $P_1$ , as shown in period  $t_1 - t_2$  in Fig. 4.

[0026] As indicated at  $t_2 - t_3$  in Fig. 4, input signal  $IN_2$  may then be switched ON. It will be noted that in the embodiment of the present invention shown in Fig. 3, switching  $IN_2$  to an ON state, i.e., low voltage, results in at least two substantially simultaneous events. The path from the high voltage source HV to output node  $n_{OUT}$  may be opened via  $P_0$ , thereby raising the voltage at output node  $n_{OUT}$  to approximately high voltage HV; and the path from the low voltage source LV to output node  $n_{OUT}$  may be closed via  $N_2$ . This simultaneous action of switching from a low voltage pre-charge to a high voltage power source may avoid contention between the sources LV and HV.

[0027] In accordance with an exemplary embodiment of the present invention shown in Fig. 3, as shown in  $t_3 - t_4$  in Fig. 4, when input  $IN_2$  signal is switched OFF, e.g., returned to a high voltage level, and input signal  $IN_1$  remains OFF, e.g., at a high voltage level, output node  $n_{OUT}$  may discharge through two paths, for example, through  $P_1$  and  $N_2$  to LV, and through  $N_0$  and  $N_1$  to ground. Thus, for example, so long as the voltage at  $n_{OUT}$  is higher than approximately the voltage of LV plus the threshold voltage of  $P_1$ ,  $n_{OUT}$  may discharge through  $P_1$  and  $N_2$ , as well as to ground through  $N_1$  and  $N_2$ . In this mode, a portion of the charge of output node  $n_{OUT}$  may optionally be returned to the low voltage source LV.

[0028] Finally, as shown in  $t_4 - t_5$  in Fig. 4, when the voltage of output node  $n_{OUT}$  reaches below LV plus the threshold voltage of  $P_1$ ,  $P_1$  shuts off, and output node  $n_{OUT}$  discharges to ground through  $N_1$  and  $N_2$ .

[0029] Reference is made to Fig. 5, which is a simplified graph of a simulation of various signals involved in the operation of the driver of Fig. 3 over time, in accordance with another method of operating an embodiment of the present invention.

[0030] As indicated at  $t_0 - t_1$ , and similar to the description of Fig. 4, in Fig. 5,  $IN_1$  and  $IN_2$  may be non-activated, setting driver 40 to an off mode, in which substantially no voltage is sourced to the output node  $n_{OUT}$ , and any voltage stored in output node  $n_{OUT}$  may be discharged and grounded through NMOS transistors  $N_0$  and  $N_1$ .

[0031] When input signal  $IN_1$  is switched ON and  $IN_2$  remains OFF, output node  $n_{OUT}$  may be pre-charged to approximately the voltage of LV

through NMOS transistor  $N_2$  and PMOS transistor  $P_1$ , as shown in period  $t_1 - t_2$  in Fig. 5, which is also shown in Fig. 4.

[0032] As indicated at  $t_2 - t_3$  in Fig. 5, when input signal  $IN_2$  is switched ON,  $IN_2$  may open the path to the high voltage source HV, and  $P_0$  may connect high voltage source HV to output node  $n_{OUT}$ , thereby raising the voltage at output node  $n_{OUT}$  to approximately high voltage HV.

[0033] In accordance with an exemplary embodiment of the present invention shown in Fig. 3, as shown in  $t_3 - t_4$  in Fig. 5, input  $IN_2$  signal may be returned to OFF mode while  $IN_1$  remains in ON mode. In this mode, output node  $n_{OUT}$  may discharge through  $P_1$  and  $N_2$  to LV, for example, as long as the voltage at  $n_{OUT}$  is higher than approximately the voltage of LV plus the threshold voltage of  $P_1$ . Thus, in this mode, a portion of the charge of output node  $n_{OUT}$  may be returned to the low voltage source LV.

[0034] Finally, as shown in  $t_4 - t_5$  in Fig. 5, input  $IN_1$  signal may be returned to OFF mode while  $IN_2$  remains in OFF mode. In this mode, output node  $n_{OUT}$  may discharge its remaining charge to ground.

[0035] It will be appreciated by persons skilled in the art that the present invention is not limited by what has been particularly shown and described herein above. For example, although particular NMOS and PMOS components have been described in the particular configuration above, it will be understood that other components and configurations may be employed within the bounds of the invention, and that the invention is not limited in this regard. For example, CMOS transistors may be used instead of PMOS and NMOS transistors, and the time diagrams of  $IN_1$  and  $IN_2$  may also be changed.